

Avinash Suresh

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EDUCATION

Rutgers University, *New Brunswick, NJ*

Masters in Electrical & Computer Engineering, GPA: 3.77/ 4.00

Aug. 2021 – May. 2023*

Relevant Coursework: Computer Architecture, VLSI Circuits and Tech, Advanced VLSI Design, Reconfigurable Computing, Analog Integrated Circuits, Advanced Systems Programming, Hands on Hardware Security

The National Institute of Engineering, *Karnataka, India*

Bachelors of Engineering in Electrical & Electronics Engineering, GPA: 7.96/ 10.00

June. 2013 – June. 2017

RESEARCH PROJECTS

Design of a 16-bit Kogge Stone Fast Adder (RTL to GDSII) / *Verilog | Aldec Riviera Pro*

Sep. 2022 – Dec. 2022

- Developed a 16-bit Kogge Stone prefix fast adder using Verilog and simulated it on EDA Playground.
- Responsible for RTL Design, Simulation, Synthesis.

4-Bit Arithmetic and Logic Unit / *Verilog | Xilinx Vivado | Xilinx Zynq – 7000*

Feb. 2022 – Apr. 2022

- Designed a 4-bit ALU in Verilog using 1-bit full adder and 4- bit ripple carry adder in Xilinx Vivado.
- Successfully implemented it using various modelling techniques on Xilinx Zynq-7000.

UART communication Protocol *Xilinx Vivado | Xilinx Zynq - 7000*

Feb. 2022 – Apr. 2022

- Implemented an UART communication protocol to transmit data between an FPGA board and a computer using VHDL programming.
- Develop and implement testing procedures.

DRAM memory hierarchy *Python*

Sep. 2021 – Dec. 2021

- Leveraged Python to develop a L1-L2-DRAM memory hierarchy system with L1 cache direct mapping and L2 cache set associativity.
- It covers basic functions as managing cache hit and miss for reading/writing data.

WORK EXPERIENCE

Schindler Elevator Corporation, *NJ, USA*

Electrical Engineer

Sep. 2022 – May 2023

- Developed and maintained **Python**-based applications for data analysis and visualization.
- Created a **Heatmap program** that analyzes call volume data based on the principles of extract, transform, load (ETL) and presents it in a more logical format using dictionaries, NumPy, and Pandas.
- Developed and maintained Python-based web applications using the **Django web framework**.
- Created a web application for reserving lab equipment using Python and Django.
- Interfaced the web application with a touch screen display using Raspberry Pi's tiny core OS. Developed and maintained **SQL databases** using Django's ORM.

Vedanta Aluminum Limited, *Odisha, India*

Electrical Engineer

August. 2017 – July. 2019

- Troubleshoot and diagnose electrical equipment failures and implement corrective actions.
- Maintenance of **ABB VFD** motor controllers, Pneumatic valves, and thermocouples.
- Worked on the slab casting project for 6 months and acquired skills in PLC programming using Ladder Logic, Structured text Language, on various PLC brands including **Allen Bradley, Rockwell Automation and Siemens**.
- Leveraged PLC and C++ programming skills and designed a PLC-based water control, furnace control and Casting Panel control systems.
- Designed and developed PID controllers in **Embedded C** for furnace heaters and tested for **hardware in loop** using MATLAB simulations.
- Contributed to the project winning the prestigious **CEO Kitty award** in FY-2018-19.
- Developed a PLC based Control System for **Nitrogen Generation Plant** in the company resulting in 25% increase in the billet production.

SKILLS

Languages: PLC Programming, Verilog, VHDL, C++, Python, Object Oriented Programming, Embedded C, Socket Programming, HTML, CSS, JavaScript, Node.js, Bootstrap5.

Databases: SQLite3, SQL, Mango DB.

Web Framework: Django 4.1, Angular

Engineering Tools: Xilinx Vivado, EDA Playground, MATLAB, PSpice, Simple Scalar, Mininet, Wireshark.

Software Tools: Git, Docker, VScode, Anaconda Navigator, PyTorch, JIRA, Terraform, Ansible.

Hardware: Atmega 16, Atmega 32, 8051 uC, Xilinx Zynq-7000, Arduino, Raspberry Pi.

Platforms: Linux, Windows.