**A.E. 'Chip' BURNS**
**Senior Embedded Software/Firmware/Hardware Engineer**
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**ACADEMICS:** B.S.M.E., Cum Laude, Univ. of Maryland, College Park, MD

**APPLICABLE EXPERIENCE:**

- 20+ years C/C++ software/firmware experience.
- 20+ years embedded development experience on 8/16/32-bit processors: ARM Cortex M0/M0+/M3/M33, MSP430, PIC, Coldfire, 80186/486, 8051/DS80C320, 68k & Z180 platforms.
- Experienced with both bare-metal and RTOS-based systems
- Design of device drivers for UART, SPI, I2C, internal ADCs/DACs, DMA, Timers, digital I/O.
- Experienced with GIT, CVS, SVN and other proprietary version control tools.
- 9 years RTOS (uC/OS-II, RTXC, SMX) experience including OS porting.
- Experienced in design of systems architecture, device drivers and middleware.
- Toolchains: IAR, JTAG/ICE, Visual Studio, MPLAB, CodeWarrior, Keil, Quartus-II, Xilinx ISE.
- Experienced with electronics and electrical components, digital & analog (schematic capture & layout) including design of 8- & 32-bit CPU systems ('51, ARM7, MSP430), design of gain/buffer/filter stages for analog inputs, design of interface(s) to 8/12/16-bit A/D & D/A converters, gain stages for analog outputs, LCDs, stepper motor controllers/ quad-counters, comparators & misc. digital I/O.
- Development of mathematical algorithms/numerical methods for data reduction of sensor inputs, e.g. A/D (FFT & linear), laser photo-diode detectors, 6-axis force sensing, machine-vision.
- Continuous use of diagnostic electronics including analog and digital oscilloscopes (TEK), CANalyzer, In-Circuit-Emulators and RS-232 analyzers.

**WORK HISTORY:**

4/2022 - 12/2022 EMBEDDED FIRMWARE ENGINEER, CQENS, Aptos, CA. Developing a "Heat not Burn" device for dispensing various medications through the pulmonary system.

- **Designed system architecture** to include module & task definitions and a queuing system for passing data between tasks. Modules included on-chip DMA, 12-bit ADC, I2C, SPI & UART components, as well as off-chip RTC, Temperature, Pressure, Battery Charging and expansion digital I/O.
- **Designed/implemented drivers** for DMA/ADC to facilitate continuous data acquisition via internal 12-bit ADC @ 10kHz. Developed buffering system to transfer 512-byte blocks of data into post-processing functions to drive PWM.
- **Designed/implemented drivers** for I2C/SPI/UART to interface with off-chip sensors and text-based UI.
- **Designed/implemented all middle-ware** for process control and time management of all tasks/modules.

7/2016 - 7/2019 EMBEDDED FIRMWARE ENGINEER, NXP, San Jose, CA, developed bare-metal drivers and middle-ware for demonstration and/or test code on multiple ARM/Cortex processors (M33/M3/M0/M0+) over a wide variety of peripherals (USART, SPI, I2C, DMA, ADC, COMP, DAC, Timers, GPIO, RTC, Watchdog etc.) and system resources (e.g. Power, I/O mux). Examples include:

- **Reduced M33 sleep current** by engaging Reverse Body Bias, explicitly shutting off all clock muxes/peripheral clocks, all RAM (5 MB) and overriding boot/default power sinks (RTC, XTAL etc.) in sleep mode.
- **Implemented 8 simultaneous USARTs @ 1Mbit using DMA** to constantly transfer RAM-to-Tx and Rx-to-RAM with no CPU involvement. Repeated using SPI @ 20Mbit and I2C @ 400kHz.
- **Experience with small (16k Flash/2k SRAM) processors** developing serial, GPIO, comparators, level-shifters, Programmable Logic Unit (PMU), etc.
- **Developed Rapid-Deployment Architecture** to quickly transition between processor families and devices. Three-tiered system implemented a layer for basic IP, family-specific and devices-specific layers. Common top-level interface allowed for code re-use and commonality across devices of different families.
- **Implemented various Wake up configurations** including simple pin interrupts and schemes utilizing serial wake-up sources (USART/SPI/I2C). Some implementations allowed for serial devices + DMA to perform data transfers in sleep mode without waking the CPU.
- **Implemented 2 different PLL engines** fixed- and fractional-frequency.
- **Utilized event logging for debugging.** Event logs contained event ID, flexible buffers for event data and time stamping as required.
- **Ported drivers between various NXP LPC processors** (ARM/Cortex M0/M4) including UART, Timers, GPIO, SPI, I2C etc. Adapted chip-level header files to different memory layouts; also updated driver interfaces via SYSCON (clocks, PLL, power etc.) and peripheral-specific memory mapping.

9/2015 - 12/2015 EMBEDDED FIRMWARE CONSULTANT, Altierre, San Jose, CA

- **Developed code for Embedded core** (FPGA-based) MSP430 using GCC in Cygwin environment. Maintained make file for all source files.
- **Developed drivers** for DMA and Digital I/O for core (FPGA-based) MSP430. Implemented both internal (memory⇨memory) and external (SPI) DMA.
- **Developed drivers** for external Flash (SPI) including block erase, sequential write, sequential read, status read and sector protect/unprotect.
- **Modified linker script** to locate RAM, ROM and interrupt vectors for the processor.

12/2013 - 3/2015 SELF-EMPLOYED, Design and manufacture of accessories for motorcycles.

- **Designed battery + inverter** to provide 420W·h of 120VAC from 12VDC, rechargeable.
- **Designed novel luggage rack** to take advantage of unused space.

7/2013 - 11/2013 EMBEDDED FIRMWARE CONSULTANT, Adaptrum, San Jose, CA

- **Maintained Remote Process Control interface** in CCS5 for Cortex A8/AM335x. Interface communicated data/control to Ethernet communications from remote host.

- **Built I2C Controller in PRU** written in PRU pseudo-assembler. Used PRU shared memory as interface from Cortex to PRU, used L4 OCP interface to access I2C peripherals from PRU

8/2012 - 4/2013 SENIOR FIRMWARE ENGINEER, Abbott Diagnostics, Santa Clara, CA.

- **Re-designed System Architecture** from static, flat, hi-maintenance to dynamic, hierarchical lo-maintenance; introduced simple state machines and state machine concepts.

- **Developed DAC/ADC code** to write/read internal (register) and external (SPI) DACs and ADCs.

- **Developed scripts and descriptors in QNX** for proprietary device control used across multiple platforms.

- **Awarded** for delivering firmware to meet project milestones on schedule.

8/2010 - 12/2011 SENIOR FIRMWARE ENGINEER, Snapon Diagnostics, San Jose, CA.

- **Designed/developed GUI interface** for Snap-on automotive diagnostic tools. Re-engineered flawed GUI implementation; developed parallel-track code to demonstrate to improved methodology to management without disturbing production code. New approach optimized code for speed/efficiency; achieved buy-in from management. Provided documentation and instruction to engineers from India to Ireland for implementing new approach.
- **Invented new method of touch-screen control** for navigating on the screen. Patent pending.

8/2008 - 8/2010 SENIOR FIRMWARE ENGINEER, MedTech Development, Sunnyvale, CA.

- **Designed MSP430F54xx drivers** for USCI (SPI,UART,I2C), ADC, DMA, Timers and PMM. Driver APIs included instantiation, configuration and usage (Start/Enable, Read/Write, Put/Get) functions. Drivers ensured resource availability and provided resource locks.

- **Systems Design of Life-Shirt Data Acquisition Processor** using an MSP430F5438 @ 16Mhz. System design included data acquisition scheme, background/foreground data transfer and communications mechanisms (double-buffering, semaphores), data post-processing, output buffering and communications protocol (serial) for upload to host processor.

- **Developed 240kS/s ADC acquisition/analysis system** on MSP430 using Timer B to trigger 12 channels of 12-bit data @ 50$\mu$sec (20kHz). Used DMA to transfer ADC data to RAM. Data was (1) post-processed and buffered for subsequent SPI transfer to host or (2) raw data was transferred via DMA to a secondary SPI port for diagnostics (@ 4Mbit).

- **Systems design** of medical devices including development of Design Input Requirements (DIR), High Level Design (HLD) and Detailed Design (DD) documents.

- **Design/development** of human implantable pump including radio-controlled operation and magnetic resonance power transfer, PIC18F45J10 processor, Salvo RTOS.

- **Design/development** of wearable health monitor including heart rate, breath rate, motion detection (accelerometer) and body temperature, both wired and wireless (Bluetooth, ZigBee) as well as Data Center communications via GSM.

6/2006 - 12/2007 EMBEDDED SOFTWARE/FIRMWARE CONSULTANT, Ambios Technology, Santa Cruz, CA. Santa Cruz, CA.

- **Systems design** (elect/layout/software/firmware) of an ARM7-based profiler controller. Designed software architecture including all control code in C/C++ and programmable logic in Verilog. CPU controlled all sub-systems via a Xilinx FPGA.
- **Ported uC/OS-II RTOS** to ARM7 target; implemented semaphores for event-based control and mailboxes/queues for lower priority inter-process communications.
- **Implemented USB 2.0** including 4-port hub for PC comm to both the target (ARM7) as well as a USB camera downstream.
- **Implemented SPI** comm.to 1x12 and 2x16-bit serial DACs, 16-bit serial ADC and stepper motor controllers. System implemented digital servo control, multiple analog control channels w/ feedback.
- **Designed stepper controllers** using Silicon Labs C8051F133 processor.
- **Implemented RS-232** comm to servo motor controller and a digital thermometer.
- **Designed all electronics** as well as component specification, layout and fab.

6/2006 - 9/2006 EMBEDDED SOFTWARE/FIRMWARE CONSULTANT, Synaptics, Santa Clara, CA. Designed $I^2C$ driver (master) for ARM7 interface to One-Touch demonstration system.

7/2005 - 11/2005 EMBEDDED SOFTWARE/FIRMWARE CONSULTANT, ZK Cell Test, Santa Clara, CA. Designed architecture/code for drive-test network measurement detecting various cell-phone events (CDMA, GSM, TDMA) and generating audio alert outputs for those events. Implemented RTOS (RTXC) tasks/queues/semaphores for generating output to remote hardware (speaker). Wrote utility code to translate .wav files into useable audio data for download to target. Assisted in firmware design for FPGA comm (register layout, cmd/data formatting) via serializer/deserializer.

4/2003 - 6/2005 SENIOR EMBEDDED SYSTEMS ENGINEER, Ambios Technology, Santa Cruz, CA Designed embedded software/hardware for Ambios XP2 profilometer.

+• **Installed 2-axis motion control** and mapping algorithm to enable automated positioning of X-Y stages on profiler product using homogeneous transforms. Mapping enabled 3-D representation of data from multiple parallel scans accurate to 10 microns (limit of stepper motor accuracy).

- **Restored non-functional consultant-provided source files to stable,** determined source C code did not match PCB layout and repaired source code (Keil C compiler for Cypress AN2131), repaired $I^2C$ interface (Verilog HDL) between CPU & FPGA (Quartus II for Altera 10K). Updated/maintained USB 2.0 I/F to host PC including building device driver w/ Windows DDK to auto-detect the target. Brought schematics up to date and consistent with Gerber files (including B.O.M. and netlist).
- **Transferred optical scan product** including circuit re-design (analog) and porting of application from Win98 environment to WinXP environment (Visual C++.NET).
- **Maintained/improved** GUI front end in Visual Basic.
- **Wrote specification for mechanical transfer function of instrument** to enable proper diagnostics of failure modes.

- **Installed QVCS archiving software** to manage revision changes.

2/1999 - 2/2003 STAFF SOFTWARE ENG, **Asyst Technology,** Fremont, CA.
Designed embedded software/hardware for wafer-fab processing robots and pre-aligners:

- **Implemented distributed servo-based control** system for 4-axis robot, upgrading from a single-point control architecture. Included design of new architecture of robots and pre-aligners in ISR based (DOS 16-bit) & multi-threaded/tasked (WinCE 32-bit) environments, 80186 &80486 processors. Design of software architecture (OOD), writing code, measuring performance and optimization.

- **Wrote/maintained re-usable objects (C/C++)** which performed various functions including buffered data acquisition, data reduction, digital I/O, serial communications & motion control. (servo and stepper). Pre-defined architecture provided for all objects to be generically creatable by an Object Request Broker (ORB).

# Chip Burns

- Scotts Valley, CA, US

## Contact Information


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- 8315152310


## Work History

### Total Work Experience: 17 years

- **EMBEDDED FIRMWARE ENGINEER CQENS**
  Apr 01, 2022
- **SENIOR FIRMWARE ENGINEER NXP**
  Aug 01, 2016
- **SOFTWARE/FIRMWARE CONSULTANT Altierre**
  Nov 01, 2015
- **Owner BMA**
  Dec 01, 2013
- **SENIOR FIRMWARE ENGINEER Adaptrum**
  May 01, 2013
- **SENIOR FIRMWARE ENGINEER Abbott Diagnostics**
  Jun 01, 2012
- **SENIOR FIRMWARE ENGINEER Snapon Diagnostics**
  Jan 01, 2010

- **SENIOR FIRMWARE ENGINEER Medtech**
  Jan 01, 2008

- **SOFTWARE/FIRMWARE CONSULTANT Ambios**
  Jan 01, 2006

## Education

- **Bachelors** | University of Maryland

## Skills

- **c** - 20 years
- **firmware** - 15 years
- **jtag** - 15 years
- **device drivers** - 12 years
- **c++** - 10 years
- **visual studio** - 10 years
- **arm** - 8 years
- **i2c** - 8 years
- **rtos** - 8 years
- **spi** - 8 years
- **uart** - 8 years
- **adc** - 7 years
- **dac** - 5 years
- **ucos** - 5 years
- **freertos** - 3 years
- **microchip** - 2 years
- **git** - 1 years
- **nxp** - 6 years
- **power management** - 3 years
- **svn** - 2 years
- **visual basic** - 5 years
- **cvs** - 8 years
- **verilog** - 2 years
- **rational rose** - 2 years

## Work Preferences

- Likely to Switch: True
- Willing to Relocate: False
- Travel Preference: 0%
- Work Authorization:
    - US
- Work Documents:
    - US Citizen
- Desired Hourly Rate: 80+ (USD)
- Desired Salary: 150,000+ (USD)
- Security Clearance: False
- Third Party: False
- Employment Type:
    - Full-time
    - Contract - W2
    - Contract to Hire - W2

## Profile Sources

- Dice: https://www.dice.com/employer/talent/profile/59863c0128f71d993b7e3c1625da2365